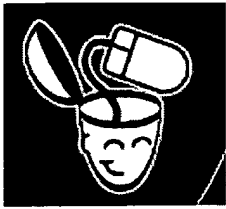


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-	3516	((multi multiple dual plural) adj1 (port ported)) adj2 (cache memory RAM)).ti,ab.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/06 11:35
-	559	((multi multiple dual plural) adj1 (port ported)) adj2 (cache memory RAM)).ti,ab.) and processor and RAM	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/05 14:50
-	480	((multi multiple dual plural) adj1 (port ported)) adj2 (cache memory RAM)).ti,ab.) and processor and RAM) and @ad < "20000612"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/04 18:18
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-	480	((multi multiple dual plural) adj1 (port ported)) adj2 (cache memory RAM)).ti,ab.) and processor and RAM) and @ad < "20000612"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/05 14:11
-	480	((multi multiple dual plural) adj1 (port ported)) adj2 (cache memory RAM)).ti,ab.) and processor and RAM) and @ad < "20000612"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/05 14:16
-	48	((multi multiple dual plural) adj1 (port ported)) adj2 (cache memory RAM)).ti,ab.) and processor and RAM) and @ad < "20000612") and (PLD FPGA EEPROM PROM)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/05 14:38
-	2	4769642.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/05 14:38
-	3516	((multi multiple dual plural) adj1 (port ported)) adj2 (cache memory RAM)).ti,ab.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/05 14:52
-	3036	((multi multiple dual plural) adj1 (port ported)) adj2 (cache memory RAM)).ti,ab.) not (((multi multiple dual plural) adj1 (port ported)) adj2 (cache memory RAM)).ti,ab.) and processor and RAM) and @ad < "20000612")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/05 14:52
-	570	((multi multiple dual plural) adj1 (port ported)) adj2 (cache memory RAM)).ti,ab.) not (((multi multiple dual plural) adj1 (port ported)) adj2 (cache memory RAM)).ti,ab.) and processor and RAM) and @ad < "20000612")) and processor	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/05 14:52

-	719	((((multi multiple dual plural) adj1 (port ported)) adj2 (cache memory RAM)).ti,ab.) not ((((((multi multiple dual plural) adj1 (port ported)) adj2 (cache memory RAM)).ti,ab.) and processor and RAM) and @ad < "20000612")) and (microprocessor micro-processor processor)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/05 14:53
-	109	((((multi multiple dual plural) adj1 (port ported)) adj2 (cache memory RAM)).ti,ab.) not ((((((multi multiple dual plural) adj1 (port ported)) adj2 (cache memory RAM)).ti,ab.) and processor and RAM) and @ad < "20000612")) and (microprocessor micro-processor processor) and ((arbitrate arbitration access) same RAM)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/05 14:55
-	50	((((multi multiple dual plural) adj1 (port ported)) adj2 (cache memory RAM)).ti,ab.) not ((((((multi multiple dual plural) adj1 (port ported)) adj2 (cache memory RAM)).ti,ab.) and processor and RAM) and @ad < "20000612")) and (microprocessor micro-processor processor) and ((arbitrate arbitration access) same RAM)) and @ad < "20000612"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/05 18:10
-	2	5802579.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/05 16:14
-	18	configurable adj1 SRAM	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/05 18:12
-	12	(configurable adj1 SRAM) and @ad<20000612	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/05 18:12
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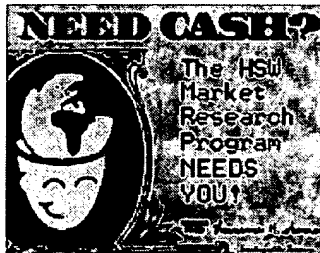
EPROM

Working with ROMs and PROMs can be a wasteful business. Even though the inexpensive per chip, the cost can add up over time. **Erasable programmable memory (EPROM)** addresses this issue. EPROM chips can be rewritten many times. Erasing an EPROM requires a special tool that emits a certain frequency of ultraviolet light. EPROMs are configured using an EPROM programmer that provides various specified levels depending on the type of EPROM used.

Once again we have a grid of columns and rows. In an EPROM, the cell at each intersection has two transistors. The two transistors are separated from each other by a thin oxide layer. One of the transistors is known as the **floating gate** and the other as the **control gate**. The floating gate's only link to the row (**wordline**) is through the control gate. As long as this link is in place, the cell has a value of 1. To change the value to 0, a special process called **Fowler-Nordheim tunneling** is used. **Tunneling** is used to allow the placement of electrons in the floating gate. An electrical charge, usually 10 to 20 volts, is applied to the floating gate. The charge comes from the column (**bitline**), enters the control gate and drains to a ground.

This charge causes the floating-gate transistor to act like an electron gun. The electrons are pushed through and trapped on the other side of the thin oxide layer. This creates a negative charge. These negatively charged electrons act as a barrier between the control gate and the floating gate. A device called a **cell sensor** monitors the level of electrons passing through the floating gate. If the flow through the gate is greater than a certain threshold, the charge, it has a value of 1. When the charge passing through drops below a certain percent threshold, the value changes to 0. A blank EPROM has all of the gates set to giving each cell a value of 1.

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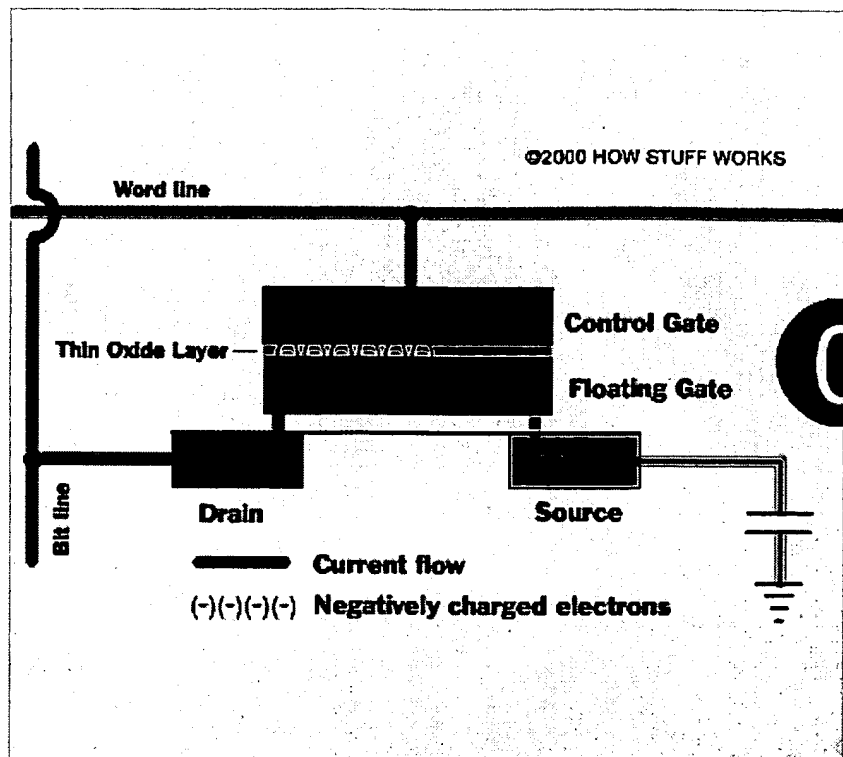
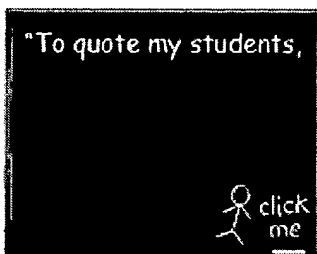


Figure 3

To rewrite an EPROM, you must erase it first. To erase it, you must supply a voltage strong enough to break through the negative electrons blocking the floating gate. In a standard EPROM, this is best accomplished with UV light at a frequency of 254 nm. This particular frequency will not penetrate most plastics or glasses, each EPROM has a quartz window on top of it. The EPROM must be very close to the eraser's lamp within an inch or two, to work properly.

An EPROM eraser is not selective, it will erase the entire EPROM. The EPROM is removed from the device it is in and placed under the UV light of the EPROM eraser for several minutes. An EPROM that is left under too long can become over-erased; in this case, the EPROM's floating gates are charged to the point that they are unable to hold any electrons at all.


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